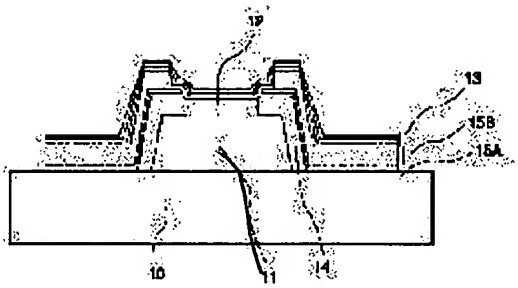
THIN-FILM TYPE ELECTRON SOURCE AND DISPLAY DEVICE USING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a structure of which can be hardly cut off the electric connection between an upper electrode and an upper electrode bus line by forming the upper electrode and the upper electrode bus line having the thinned connecting side on a protective insulating layer, and connecting the upper electrode to its thinned part, while covering the upper electrode bus line.



SOLUTION: In a cross section equivalent to a single electron source of a thin-film type electron source, an opening part of a thin upper electrode bus line lower layer 15A approaches an electron-emitting part surrounded by a protective insulating layer 14 more than an opening part of an upper electrode bus line upper layer 15B. An upper electrode is formed of the upper electrode bus line upper layer 15B, the upper electrode bus line lower layer 15A, the protective insulating layer 14 and an insulating layer 12 of the electron emitting part surrounded by it. Since the upper electrode bus line lower layer 15A is thin, the upper electrode 13 is hardly disconnected in its step difference part, and no matter how steep a step difference of the upper electrode bus line upper layer 15B is, electrical contact with an upper electrode bus line is maintained. Therefore, the upper layer 15B may be thickened to any extent.

LEGAL STATUS

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Claim(s)]

[Claim 1] The electron emission section which the laminating was carried out in the order of a lower electrode, an insulating layer, and an up electrode on the insulating substrate and this insulating substrate, and has been arranged in the shape of a matrix, It has the up electrode bus line to which the connection side between a protection insulating layer thicker than the above-mentioned insulating layer formed in the perimeter of the above-mentioned insulating layer and the above-mentioned up electrode formed on this protection insulating layer is thin. the above-mentioned up electrode -- the above-mentioned up electrode bus line -- a bonnet and the above -- the thin film mold electron source characterized by having connected with the part which is thin.

[Claim 2] the above-mentioned up electrode bus line -- the above -- the thin film mold electron source according to claim 1 characterized by consisting of a cascade screen of the lower layer film containing the part which is thin, and the upper film formed on this lower layer film, and the top-face section of the above-mentioned lower layer film consisting of one film chosen from the groups which consist of Pt, Au, Ir, Rh, and Ru.

[Claim 3] The above-mentioned insulating layer is a thin film mold electron source according to claim 1 or 2 characterized by consisting of what carried out the laminating of the insulator film and the semi-conductor film.

[Claim 4] The above-mentioned insulating layer is a thin film mold electron source according to claim 1 or 2 characterized by having the porosity semi-conductor.

[Claim 5] The indicating equipment with which the substrate with which a thin film mold electron source according to claim 1 to 4 was formed, and the face-plate which applied a fluorescent substance are characterized by to have the indicating-equipment panel by which the vacuum lock was carried out by the arrangement which the electron emitted from the above-mentioned thin film mold electron source is in charge of in the above-mentioned fluorescent substance, the lower electrode actuation circuit connected to the above-mentioned lower electrode, and the up electrode actuation circuit which were connected to the above-mentioned up electrode bus line.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention has the electron emission section of the three-tiered structure of a lower electrode-insulating-layer-up electrode, and relates to the display using the thin film mold electron source and it which emit an electron into a vacuum from an up electrode.
[0002]
[Description of the Prior Art] As a display using the cold cathode array in which cold cathode was formed on each intersection of the electrode group which intersects perpendicularly mutually, there is a field emission display (FED) indicated by JP,4-289644,A, for example. FED arranges much field emission cathode to each pixel, after it accelerates in a vacuum, irradiates a fluorescent substance and makes the field emission electron from there emit light.
[0003] On the other hand, a thin film mold electron source impresses an electrical potential difference between the lower electrode of the three-layer diaphragm structure of a lower electrode, an insulating layer, and an up electrode, and an up electrode, and makes the electron which penetrated the insulating layer according to tunneling etc. emit into a vacuum from an up electrode surface. There are an MIM (metal-insulator-metal) mold electron source which used the metal for the up electrode and the lower electrode, an MIS (metal mold-insulator-semi-conductor) mold electron source which used the semi-conductor at least for one side. The MIM electron source is shown in JP,7-65710,A, for example. Moreover, what carried out the laminating of the insulator film and the semi-conductor film on the lower electrode at this order, and constituted the insulating layer, the thing which made built-up sequence reverse or the thing constituted from a porosity semi-conductor, and the thing which oxidized the top face of a porosity semi-conductor further are also known.
[0004]
[Problem(s) to be Solved by the Invention] Compared with the field emission cathode used for FED, it has the desirable property in the display that a thin film mold electron source is strong to surface contamination, and is low etc. [of operating voltage] However, that a life is short since electric field concentrate on the insulating layer of a component edge and dielectric breakdown happens conventionally, and since [that an up electrode was thin] electric resistance was high, when a thin film mold electron source was formed in the shape of a matrix, there were problems, like the amount of electron emission within a field becomes an ununiformity. To these problems, we formed the up electrode bus line which reduces the thick protection insulating layer which prevents electric-field concentration of the insulating layer of a component edge, and wiring resistance of an up electrode, and stated structure, the manufacture approach, etc. of a thin film mold electron source that uniform electron emission was obtained in long lasting actuation and a field, by Japanese Patent Application No. No. 250279 [eight to]. An up electrode bus-line layer is covered, the up electrode layer is formed, and this structure has the description in forming the up electrode bus line which consists of a cascade screen of an up electrode bus-line layer and an up electrode layer. By adopting the structure which forms an up electrode at the end, the process damage of an insulating layer can be prevented or restored, and a reliable thin film electron source can be produced. Furthermore on an up electrode bus line and an insulating layer, it also becomes possible to produce an up electrode by self align at a protection insulating-layer top.
[0005] By the way, when producing a large-sized indicating equipment etc., since buildup of wiring resistance poses a problem, as an up electrode bus line is thick, it is better. However, if an up electrode bus line is thickened too much, the level difference of an up electrode bus-line edge will become steep, and it becomes easy to disconnect the up electrode formed from an up electrode bus line in the level difference section, and becomes easy to generate a defect.
[0006] The object of this invention is to offer the thin film mold electron source of the structure where the electrical installation between an up electrode and an up electrode bus line is hard to be severed, and the display using it.

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[0007]
[Means for Solving the Problem] The above-mentioned object forms the up electrode bus line to which the connection side with an up electrode is thin on the protection insulating layer thicker than this insulating layer formed in the perimeter of the insulating layer which constitutes the electron emission section, and can attain an up electrode by connecting with the part which is thin [a bonnet and it] about the up electrode bus line.
[0008]
[Embodiment of the Invention]
The thin film mold electron source of an example 1 is explained using example 1 drawing 1 thru/or drawing 19. A top view [in / drawing 1 / in the production process flow, drawing 2, or drawing 18 of a thin film electron source / each process] and a sectional view, and drawing 19 are the sectional views for one electron source of a thin film mold electron source.
[0009] First, in a process P1, aluminum film is formed by 300nm thickness as a thin film for lower electrode 11 creation on the substrate 10 of insulation, such as glass. formation of this aluminum film -- for example, the sputtering method, resistance heating vacuum deposition, and MBE -- law etc. is used. Next, this aluminum film is processed into the resist formation and it by photolithography in the shape of a stripe by ****** etching, and as shown in drawing 2, the lower electrode 11 is formed. Both wet etching and dry etching are possible for etching.
[0010] Hereafter, the production process of the description section of this invention which consists of an insulating layer 12, the protection insulating layer 14, up electrode bus-line lower layer 15A, up electrode bus-line upper 15B, and an up electrode 13 is described.
[0011] First, according to the process P2, as shown in drawing 3, formation voltage formed 2Oaluminum3 insulating layer 12 of 5.5nm of thickness with the anode oxidation method of 4V.
[0012] Then, as shown in a process P3 and drawing 4, the resist pattern R1 which covers the field used as the electron emission section arranged in the shape of a matrix is formed in the shape of a matrix.
[0013] Next, as shown in a process P4 and drawing 5, the protection insulating layer 14 is formed with an anode oxidation method. The part covered with the resist pattern R1 does not oxidize, but serves as as [a thin insulating layer], and serves as the electron emission section. As described above, the insulating layer is beforehand formed of the process 12, but if high formation voltage is applied, the part which is not covered with a resist pattern R1 can advance oxidation further, and can form the thick protection insulating layer 14. In this example, formation voltage was set to 50 V and the protection insulating layer 14 of 68 nm was formed. Even if it forms the thick protection insulating layer 14 by using anodic oxidation, the level difference in the boundary of the protection insulating layer 14 and an insulating layer 12 is small, and it is hard to disconnect the up electrode 13 formed behind. The resist pattern R1 exfoliates after protection insulating-layer 14 formation.
[0014] Then, the method of producing the up electrode bus line 15 which consists of up electrode bus-line lower layer 15A and up electrode bus-line upper 15B is shown.
[0015] First, the resist pattern R2 which covers the part used as the field which surrounds the electron emission section as shown in a process P5 and drawing 6, and the tooth space between the up electrode bus lines 15 is formed.
[0016] Then, the metal membrane set to up electrode bus-line lower layer 15A as shown in a process P6 and drawing 7 is formed on the whole surface. The film which carried out the laminating of a metal membrane with a strong adhesive property with a substrate 10 or an insulating layer 12 and the metal membrane to which a front face cannot oxidize easily in this order is used for the metal membrane besides set to section electrode bus-line lower layer 15A. By using the metal membrane to which a front face cannot oxidize easily, electric contact to up electrode bus-line upper 15B formed behind and the up electrode 13 can be ensured. There may not be a metal membrane excellent in the adhesive property, when the adhesive property of the metal membrane to which a front face cannot oxidize easily fills a demand. In this example, Pt was used as a metal membrane to which a front face cannot oxidize Mo easily as a metal membrane with a strong adhesive property with a substrate 10 or an insulating layer 12. To the metal membrane by which neither Cr, nor Ta, W, Nb, etc. can oxidize easily on a front face as a

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metal membrane with a strong adhesive property with a substrate 10 or an insulating layer 12, Au, Ir, Rh, Ru, etc. besides Pt are usable. Moreover, as for the thickness of the metal membrane used as up electrode bus-line lower layer 15A, it is desirable to make it as thin as possible. In this example, Mo was set to 20 nm and Pt was set to 10 nm. The level difference of up electrode bus-line 15A becomes small by this, and an open circuit of the up electrode 13 formed behind can be prevented. The metal membrane used as up electrode bus-line lower layer 15A is set to up electrode bus-line lower layer 15A of the shape of a stripe in which the field surrounding the electron emission section carried out opening by carrying out the lift off of the resist pattern R2, as shown in a process P7 and drawing 8 after that.

[0017] Up electrode bus-line upper 15B is produced by the lift-off method or the etching method. When performing processing by the lift-off method, as first shown in a process P8 and drawing 9, the resist pattern R3 which covers the part used as the field which surrounds the electron emission section and also surrounds opening of up electrode bus-line lower layer 15A, and the tooth space between the up electrode bus lines 15 is formed.

[0018] Then, as shown in a process P9 and drawing 10, the metal membrane used as up electrode bus-line upper 15B is formed on the whole surface. In this example, thickness is thickened with about 1 micrometer using aluminum of low electrical resistance materials. As low electrical resistance materials, Au besides aluminum etc. is usable. When processing it by the lift-off method, the rectilinear-propagation nature of the particle at the time of membrane formation, such as resistance heating vacuum deposition, produces the forming-membranes method by the good approach. Thereby, it is few, and film adhesion on resist pattern R3 side face becomes easy [a lift off], even when thickness is thick. By besides thickening thickness of section electrode bus-line upper 15B, reduction of the wiring resistance which is the object of up electrode bus-line 15 original is attained. Up electrode bus-line upper 15B of the shape of a stripe in which the field which surrounds the electron emission section and also surrounds opening of up electrode bus-line lower layer 15A further by the lift off of a resist pattern R3 as shown in a process P10 and drawing 11 is carrying out opening is formed after membrane formation.

[0019] When processing it by the etching method, as first shown in a process P11 and drawing 12, the resist pattern R4 which covers the field surrounding the electron emission section is formed. Next, as shown in a process P12 and drawing 13, the metal membrane used as up electrode bus-line upper 15B is formed. In this example, thickness was thickened with about 1 micrometer using aluminum. When processing it by the etching method, the approach that the rectilinear-propagation nature of the particle at the time of membrane formation, such as the sputtering method, is bad is sufficient as the forming-membranes method. Next, as shown in a process P13 and drawing 14, the field surrounding a resist pattern R4 carries out opening, and the resist pattern R5 with which the part used as up electrode bus-line upper 15B is covered is formed. Then, as shown in a process P13 and drawing 15, the metal membrane used as up electrode bus-line upper 15B is etched, and up electrode bus-line upper 15B is formed. In this case, the resist pattern R5 which covered the protection insulating layer 14, up electrode bus-line upper 15A, and the electron emission section serves as an etching stopper. After etching exfoliates resist patterns R4 and R5.

[0020] The process which finally forms the up electrode 13 is described. First, as shown in a process P14 and drawing 16, the resist pattern R6 which covers the part used as the tooth space between the up electrodes 13 is formed. It restores, in order that an insulating layer 12 may tend to receive the damage by a developer etc. here at the time of the development of a resist. Then, re-anodic oxidation of an insulating layer 12 is performed, with a resist pattern attached. Formation voltage was set to 4V in this example. Only a damage can be restored without this changing the thickness of an insulating layer 12.

[0021] Next, the metal membrane which serves as the up electrode 13 as shown in a process P16 and drawing 17 is formed. The metal membrane used as the up electrode 13 uses three layer membranes which make heat-resistant good Ir as a lower layer, and make the upper layer Au with a sufficient interlayer and electron emission effectiveness for Pt. In this example, each thickness was set to 1 nm, 2 nm, and 3 nm, and was set to 6 nm on the whole. The metal membrane which besides serves as the section electrode 13 serves as the up stripe-like electrode 13 by carrying out the lift off of the resist, as shown in a process P17 and drawing 18.

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[0022] In addition, in this example, although the up electrode formed the others and protection insulating layer 14, up electrode bus-line lower layer 15A, and up electrode bus-line upper 15B in the wrap, it is good to cover the electron emission section and up electrode bus-line lower layer 15A. [section / electron emission] In short, up electrode bus-line lower layer 15A and electrical installation should just be obtained.

[0023] Drawing 19 shows the cross section for one electron source of the thin film mold electron source manufactured as mentioned above. This structure is the characteristic structure where thin opening of up electrode bus-line lower layer 15A is close to the electron emission section surrounded by the protection insulating layer 14 from opening of up electrode bus-line upper 15B, and the up electrode is formed from up electrode bus-line upper 15B, up electrode bus-line lower layer 15A, the protection insulating layer 14, and the insulating layer 12 of the electron emission section surrounded by it. However steep up electrode bus-line lower layer 15A cannot disconnect the up electrode 13 easily due to the level difference section since it is thin, and its level difference of up electrode bus-line upper 15B may be, the electric contact to the up electrode bus line 15 is maintained. therefore, up electrode bus-line upper 15B -- without limit -- thick -- it can form -- low -- the up electrode bus line [****] 15 is realizable.

[0024] Example 2 drawing 2 thru/or 3, drawing 20, or drawing 31 explains the thin film electron source of an example 2. A top view [in / drawing 20 / in the production process flow, drawing 2 or 3, drawing 21, or drawing 30 of a thin film electron source / each process] and a sectional view, and drawing 31 are the sectional views for one electron source of a thin film mold electron source.

[0025] First, as shown in drawing 2, after forming the lower electrode 11 according to a process P21, as a process P22 showed to drawing 3, formation voltage formed 2Oaluminum3 insulating layer 12 of thickness 5.5 nm with the anode oxidation method which is 4V. As a process P23 shows to drawing 21 continuously, the resist pattern R11 which covers the part used as the tooth space between the up electrode bus lines 15 is first formed using the resist which changes with the postbake temperature after the dissolution property over a solvent developing negatives, for example, the positive type photoresist of a quinone Gia Zaid system, and postbake processing is carried out at a 140-160-degree C elevated temperature. In this case, in order to carry out heat condensation, it becomes insoluble at an acetone or alcohol and another solvent is required. As a process P24 shows to drawing 22 continuously, the resist pattern R12 which covers the electron emission section arranged in the shape of a matrix is formed in the shape of a matrix, and postbake is carried out at 70-130-degree C low temperature. Then this resist pattern R12 is meltable to an acetone or alcohol, according to a process P25, as shown in drawing 23, it uses these resist patterns R11 and R12 as a mask, it anodizes except the electron emission section, and forms the protection insulating layer 14. The thickness of the protection insulating layer 14 is controllable by formation voltage. Here, formation voltage was set to 50V and the aluminum2O3 protection insulating layer 14 of thickness 68 nm was formed.

[0026] The metal membrane set to up electrode bus-line lower layer 15A as a process P26 shows to drawing 24 below is formed. Mo etc. forms first the metal excellent in the adhesive property with a substrate 10 or an insulating layer 12, and the metal membrane used as the up electrode bus-line lower layer 15 forms continuously the metal with which front faces, such as Pt, cannot oxidize easily. As an ingredient of a metal membrane with a strong adhesive property with an insulating layer 12, Cr, Ta, W, Nb of Au, Ir, Rh, Ru, etc. besides Pt, etc. are usable as an ingredient of a metal membrane with which a front face cannot oxidize easily. The electric contact to up electrode bus-line upper 15B formed later and the up electrode 12 is securable by using these metals. Moreover, as for the thickness of the metal membrane used as up electrode bus-line lower layer 15A, it is desirable to make it as thin as possible. In this example, Mo was set to 20 nm and Pt was set to 10 nm. An open circuit of the up electrode 13 which this forms behind can be prevented. Then, as shown in a process P27 and drawing 25, by being immersed in an acetone, the lift off of the resist pattern R12 is carried out, and opening of the part equivalent to the electron emission section of the metal membrane used as up electrode bus-line lower layer 15A is removed and carried out. A resist pattern R11 remains at this time, without exfoliating.

[0027] Next, as shown in a process P28 and drawing 26, opening of a metal membrane used as up electrode bus-line lower layer 15A and the field of the perimeter are covered with a resist pattern R13.

[0028] Then, the metal membrane set to up electrode bus-line upper 15B as shown in a process P29 and drawing 27 is formed. In this example, it created with vacuum deposition using aluminum of low electrical resistance materials. Au besides aluminum etc. is usable. Thickness of the metal membrane used as up electrode bus-line upper 15B is thickened with about 1 micrometer. Thereby, reduction of the wiring resistance which is the object of up electrode bus-line 15 original is attained. By the lift off of the resist pattern R13 by the acetone, after membrane formation removes and carries out opening of the field of the part equivalent to the electron emission section of the metal membrane used as up electrode bus-line upper 15B, and its perimeter, as shown in a process P30 and drawing 28.
[0029] Although this example described only the lift-off method about the method of processing the up electrode bus-line upper layer, the etching method shown in the example 1 is also possible by the same technique.
[0030] Next, the metal membrane which serves as the up electrode 13 as shown in a process P31 and drawing 29 is formed. Three layer membranes which make heat-resistant good Ir as a lower layer, and make the upper layer Au with a sufficient interlayer and electron emission effectiveness for Pt are used for the metal membrane used as the up electrode 13. In this example, each thickness was set to 1nm, 2 nm, and 3 nm, and was set to 6 nm on the whole.
[0031] By carrying out the lift off of the resist pattern R11 of a stripe to the last, as shown in a process P32 and drawing 30, up electrode bus-line lower layer 15A, up electrode bus-line upper 15B, and the up electrode 13 are simultaneously processed in the shape of a stripe.
[0032] In addition, although the up electrode formed others and up electrode bus-line lower layer 15A and up electrode bus-line upper 15B in the wrap, since electrical installation is obtained, at least a wrap does not care about the electron emission section and up electrode bus-line lower layer 15A with this example. [section / electron emission]
[0033] The thin film electron source matrix which has the structure of this invention according to the above process is completed. Drawing 31 shows the enlarged section for one electron source of the thin film mold electron source manufactured as mentioned above. Opening of thin up electrode bus-line lower layer 15A was formed by self align on the protection insulating layer 14, and is in contact with the electron emission section, it gets down and this structure is the characteristic structure where opening of thick up electrode bus-line upper 15B is separated from the electron emission section and where the up electrode is formed from up electrode bus-line upper 15B, up electrode bus-line lower layer 15A, and the insulating layer 12 of the electron emission section. However steep up electrode bus-line lower layer 15A cannot disconnect the up electrode 13 easily due to the level difference section since it is thin, and its level difference of up electrode bus-line upper 15B may be, the electric contact to the up electrode bus line 15 is maintained. therefore, up electrode bus-line upper 15B -- without limit -- thick -- it can form -- low -- the up electrode bus line [****] 15 is realizable.
[0034] The display of an example 3 is explained using example 3 drawing 32 thru/or 36. Drawing 32 is the fragmentary sectional view of the die-length direction of the lower electrode 11 in a display panel, and has the composition that the substrate 10 in which the example 1 or the thin film mold electron source of 2 was formed, and the face-plate 110 by the side of a display counter on both sides of a spacer 60. The glass of translucency etc. is used for the face-plate 110 which becomes a display side.
[0035] First, the black matrix 120 is formed in order to raise the contrast of an indicating equipment. The black matrix 120 is arranged between fluorescent substances 114 in drawing 33.
[0036] The black matrix 120 applies to a face-plate 110 the solution which mixed PVA (polyvinyl alcohol) and an ammonium dichromate to graphite powder, and after irradiating ultraviolet rays and making a part to form the black matrix 120 in expose them, it removes a non-exposed part.
[0037] Next, red fluorescent substance 114A is formed. After irradiating ultraviolet rays and making the part which forms a fluorescent substance 114 after applying the water solution which mixed PVA (polyvinyl alcohol) and an ammonium dichromate to the fluorescent substance particle on a face-plate 110 expose them, a stream removes a non-exposed part. Thus, red fluorescent substance 114A is patternized. A pattern is patternized in the shape of [as shown in drawing 33] a stripe. This stripe pattern is an example and, of course, may also be the "RGBG" pattern which made 1 pixel constitute

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from 4 dots which approaches besides it, corresponding to the design of a display. It is made for fluorescent substance thickness to become 1.4 - two-layer extent. Similarly, green fluorescent substance 114B and blue fluorescent substance 114C are formed. as a fluorescent substance -- red -- Y2O2 S:Eu (P22-R) -- green -- Zn2SiO4:Mn -- what is necessary is just to use ZnS:Ag (P22-B) blue
[0038] Subsequently, after carrying out filming by film, such as a nitrocellulose, thickness 50-300 nm extent vacuum evaporationo is carried out, and aluminum is considered as the metal back 122 at the face-plate 110 whole. This metal back 122 works as an accelerating electrode. Then, a face-plate 110 is heated at about 400 degrees C, and the organic substance, such as filming film and PVA, is decomposed thermally. Thus, a face-plate 110 is completed.
[0039] Thus, the face-plate 110, the substrate 10, and spacer 60 which were produced are sealed. The distance between the face-plate 110-substrates 10 sets up the thickness of a spacer 60 so that it may be set to about 1-3mm. The physical relationship of a face-plate 110 and a substrate 10 is as having been shown in drawing 33. The pattern of the thin film electron source formed on the substrate 10 is made to correspond to drawing 33, and it is shown in drawing 34.
[0040] The configuration of a spacer 60 is carried out like drawing 32. Here, although the stanchion of a spacer 60 is prepared every three trains of every dot which emits light to R (red), G (green), and B (blue), and the electron emission section, the number of stanchions (consistency) may be reduced in the range which mechanical strength bears. A fabrication of a spacer 60 processes the hole of a desired configuration into electric insulating plates, such as glass with a thickness of about 1-3mm and ceramics, for example, by the sandblasting method etc.
[0041] the sealed panel is exhausted to the vacuum of 1x10-7Torr extent, and has been stopped. Thus, the display panel using a thin film electron source is completed.
[0042] Thus, in this example, about 1-3mm and acceleration voltage impressed to the metal back 122 since it is long are made as for the distance between a face-plate 110 and a substrate 10 to 3-6kV and high tension. Therefore, the fluorescent substance 114 for cathode-ray tubes (CRT) can be used for a fluorescent substance 114 as mentioned above.
[0043] Drawing 35 is the schematics to the actuation circuit of the display panel which carried out in this way and was manufactured. The lower electrode 11 is connected to the lower electrode actuation circuit 61, and connects the up electrode 13 in the up electrode actuation circuit 62. n-th lower electrode 11 Kn and m-th up electrode bus line 15 The intersection of Cm will be expressed with (n, m). The acceleration voltage 63 of about 3-6kV is always impressed to the metal back 122.
[0044] Drawing 36 shows the wave of the generated voltage of each actuation circuit. At time of day t0, since any electrode is electrical-potential-difference zero, an electron is not emitted, therefore a fluorescent substance 114 does not emit light. It sets at time of day t1, and is the lower electrode 11. About the electrical potential difference set to K1 -V1, it is the up electrode 13. The electrical potential difference which becomes +V2 is impressed to C1 and C2. Since an electrical potential difference is impressed between an intersection (1 1) and (1 or 2) lower electrode 11-up electrodes 13 (V1+V2), if (V1+V2) is set up more than electron emission starting potential, from the thin film mold electron source of these two intersections, an electron will be emitted into a vacuum. After being accelerated with the acceleration voltage 63 impressed to the metal back 122, the emitted electron collides with a fluorescent substance 114, and makes a fluorescent substance 114 emit light. In time of day t2, if the electrical potential difference which becomes 11 lower electrodeK2 -V1 is impressed and the electrical potential difference set to C1 of the up electrode 13 V2 is impressed, an intersection (2 1) will light up similarly. Thus, the image or information on desired can be displayed by changing the signal impressed to the up electrode 13. Moreover, an image with gradation can be displayed by changing suitably the magnitude of the applied voltage V1 to the up electrode 13.
[0045] In the indicating equipment of this invention, the up electrode bus line 15 of a display panel can form thickly up electrode bus-line upper 15B, and since it is rear-spring-supporter low resistance, the image display of brightness also with a uniform large-sized indicating equipment is obtained by the panel overall length. Furthermore an open circuit of the up electrode 13 can be prevented, defect generating of dot omission etc. is lost, and improvement in the yield of a panel fabrication can be

realized.
[0046]
[Effect of the Invention] Since it becomes possible to thicken thickness of the thick part of an up electrode bus line according to this invention, the image display of brightness also with the uniform display panel of big size is realizable. Moreover, defects, such as dot omission resulting from an open circuit of an up electrode, decrease in number, and a yield improves.

[Translation done.]

[Brief Description of the Drawings]
[Drawing 1] It is process flow drawing showing the manufacture approach of the thin film mold electron source of the example 1 of this invention.
[Drawing 2] It is the top view (a) and sectional view (b) of a lower electrode formation phase in drawing 1 .
[Drawing 3] It is the top view (a) and sectional view (b) of an insulating stratification phase in drawing 1 .
[Drawing 4] It is the top view (a) and sectional view (b) of a resist pattern R1 formation phase in drawing 1 .
[Drawing 5] It is the top view (a) and sectional view (b) of a protection insulation stratification phase in drawing 1 .
[Drawing 6] It is the top view (a) and sectional view (b) of a resist pattern R2 formation phase in drawing 1 .
[Drawing 7] It is the top view (a) and sectional view (b) of a metal membrane membrane formation phase used as the up electrode bus-line lower layer in drawing 1 .
[Drawing 8] It is the top view (a) and sectional view (b) of an up electrode bus-line lower layer formation phase in drawing 1 .
[Drawing 9] It is the top view (a) and sectional view (b) of a resist pattern R3 formation phase in drawing 1 .
[Drawing 10] It is the top view (a) and sectional view (b) of a metal membrane membrane formation phase used as the up electrode bus-line upper layer in drawing 1 .
[Drawing 11] It is the top view (a) and sectional view (b) of an up electrode bus-line up stratification phase in drawing 1 .
[Drawing 12] It is the top view (a) and sectional view (b) of a resist pattern R4 formation phase in drawing 1 .
[Drawing 13] It is the top view (a) and sectional view (b) of a metal membrane membrane formation phase used as the up electrode bus-line upper layer in drawing 1 .
[Drawing 14] It is the top view (a) and sectional view (b) of a resist pattern R5 formation phase in drawing 1 .
[Drawing 15] It is the top view (a) and sectional view (b) of an up electrode bus-line up stratification phase in drawing 1 .
[Drawing 16] It is the top view (a) and sectional view (b) of a resist pattern R6 formation phase in drawing 1 .
[Drawing 17] It is the top view (a) and sectional view (b) of an up electrode membrane formation phase in drawing 1 .
[Drawing 18] It is the top view (a) and sectional view (b) of an up electrode formation phase in drawing 1 .
[Drawing 19] It is the sectional view for one electron source of the thin film mold electron source of the example 1 of this invention.
[Drawing 20] It is process flow drawing showing the manufacture approach of the thin film mold electron source of the example 2 of this invention.
[Drawing 21] It is the top view (a) and sectional view (b) of a resist pattern R11 formation phase in drawing 20 .
[Drawing 22] It is the top view (a) and sectional view (b) of a resist pattern R12 formation phase in drawing 20 .
[Drawing 23] It is the top view (a) and sectional view (b) of a protection insulation stratification phase in drawing 20 .
[Drawing 24] It is the top view (a) and sectional view (b) of a metal membrane membrane formation phase used as the up electrode bus-line lower layer in drawing 20 .
[Drawing 25] It is the top view (a) and sectional view (b) of an up electrode bus-line lower layer formation phase in drawing 20 .

h g cg b eb cg e e

[Drawing 26] It is the top view (a) and sectional view (b) of a resist pattern R13 formation phase in drawing 20 .
[Drawing 27] It is the top view (a) and sectional view (b) of a metal membrane membrane formation phase used as the up electrode bus-line upper layer in drawing 20 .
[Drawing 28] It is the top view (a) and sectional view (b) of an up electrode bus-line up stratification phase in drawing 20 .
[Drawing 29] It is the top view (a) and sectional view (b) of an up electrode membrane formation phase in drawing 20 .
[Drawing 30] It is the top view (a) and sectional view (b) of an up electrode formation phase in drawing 20 .
[Drawing 31] It is the sectional view for one electron source of the thin film mold electron source of the example 2 of this invention.
[Drawing 32] It is the fragmentary sectional view of the die-length direction of the lower electrode in the display panel of the display of the example 3 of this invention.
[Drawing 33] It is a top view in the phosphor-screen location in drawing 32 .
[Drawing 34] It is the top view of the substrate in drawing 32 .
[Drawing 35] They are the schematics of the display panel and actuation circuit in the display of the example 3 of this invention.
[Drawing 36] It is the driver voltage wave form chart of the display of the example 3 of this invention.
[Description of Notations]
10 ... A substrate, 11 ... A lower electrode, 12 ... Tunnel insulating layer, 13 ... An up electrode, 14 ... A protection insulating layer, 15 ... Up electrode bus line, 15A ... An up electrode bus-line lower layer, 15B ... Up electrode bus-line upper layer, R1 ... The resist pattern which covers the electron emission section in an example 1, R2 ... The resist pattern for up electrode bus-line lower layer processing in an example 1, R3 ... The resist pattern for the up electrode bus-line upper lift-off processing in an example 1, R4 ... The resist pattern for electron emission section protection in an example 1, R5 ... The resist pattern for the up electrode bus-line upper etching processing in an example 1, R5 ... The resist pattern for up electrode formation in an example 1, R11 ... The resist pattern which covers the electron emission section in an example 2, R12 ... The resist pattern for up electrode bus-line processing in an example 2, R13 ... The resist pattern for opening processing of the up electrode bus-line upper layer in an example 2, 60 [... Acceleration voltage, 110 / ... A face-plate, 114 / ... A fluorescent substance, 120 / ... A black matrix, 122 / ... Metal back] ... A spacer, 61 ... A lower electrode actuation circuit, 62 ... An up electrode actuation circuit, 63

[Translation done.]

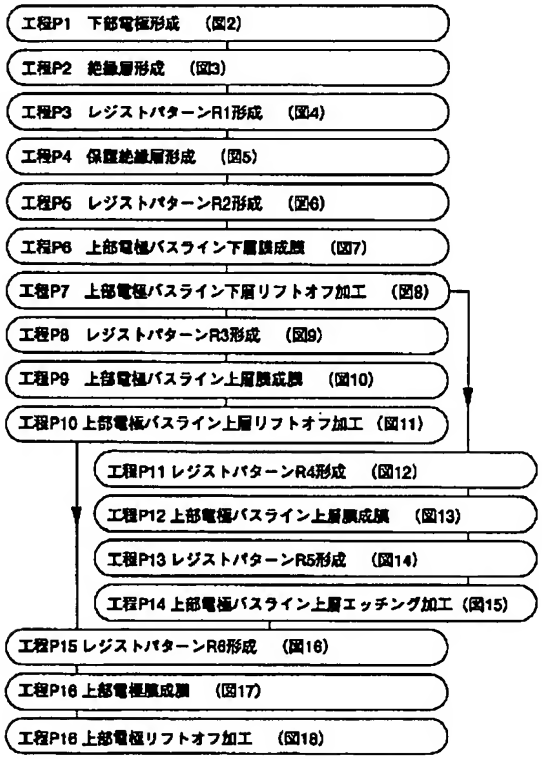
h g cg b eb cg e e

* NOTICES *

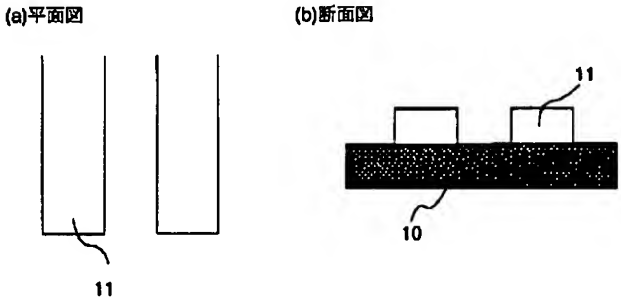
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]
図1



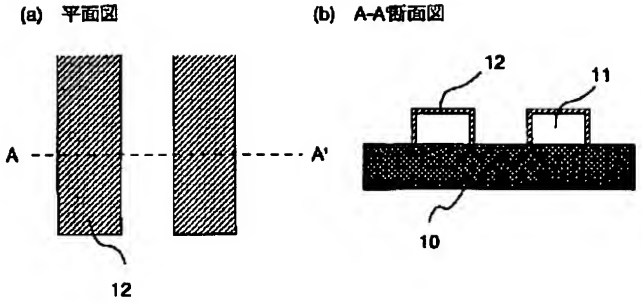
[Drawing 2]
図2



[Drawing 3]

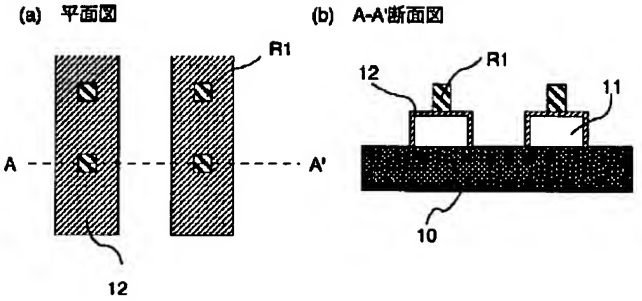
h g cg b eb cg e e

図3



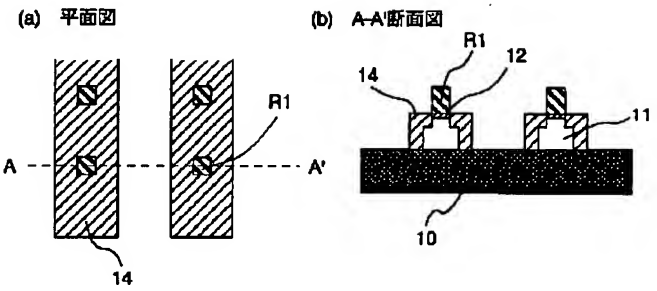
[Drawing 4]

図4



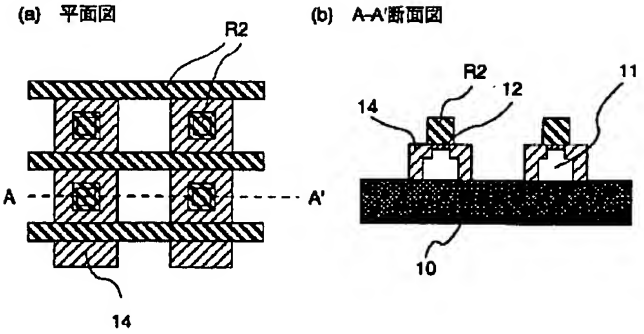
[Drawing 5]

図5



[Drawing 6]

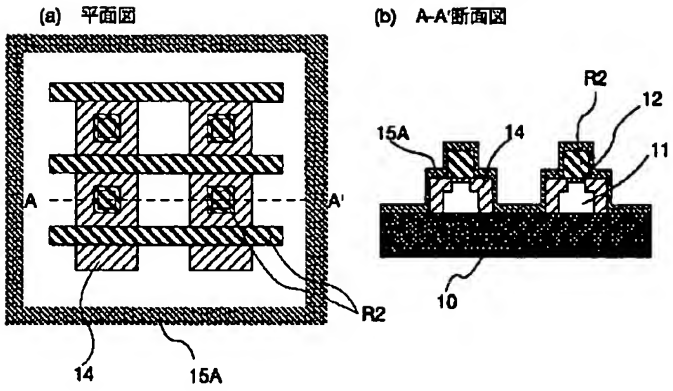
図6



[Drawing 7]

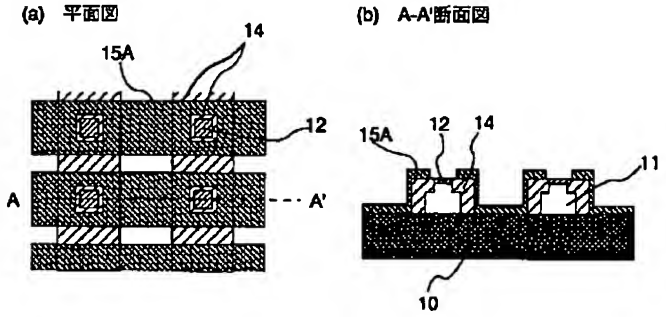
h g cg b eb cg e e

図7



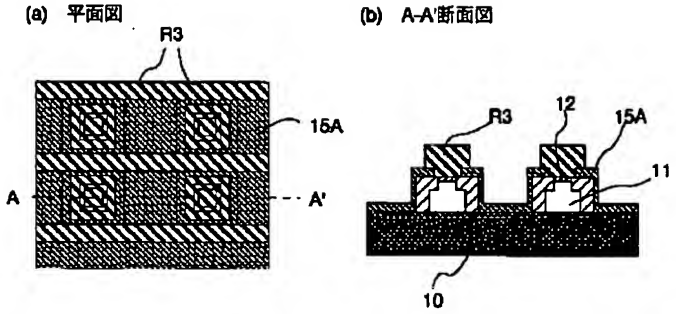
[Drawing 8]

図8



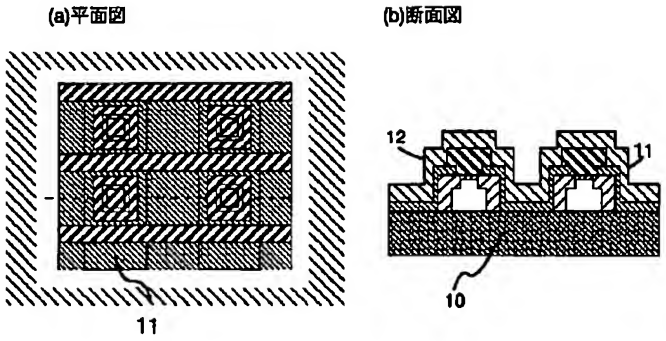
[Drawing 9]

図9



[Drawing 10]

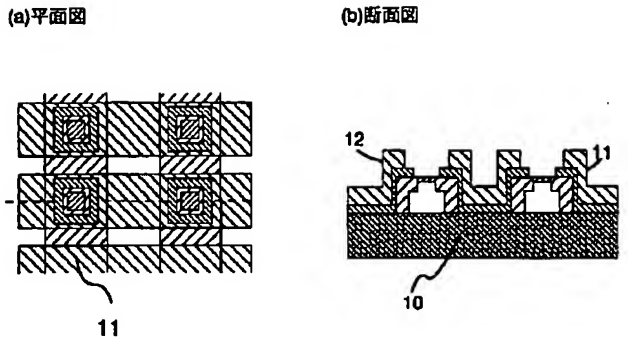
図10



[Drawing 11]

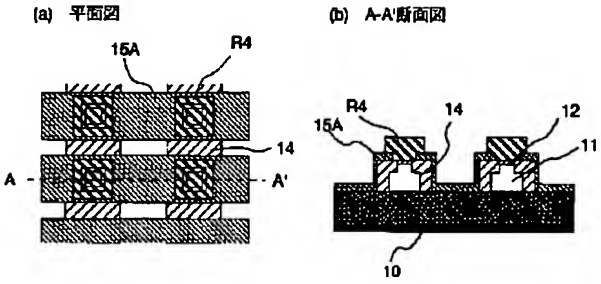
h g cg b eb cg e e

図11



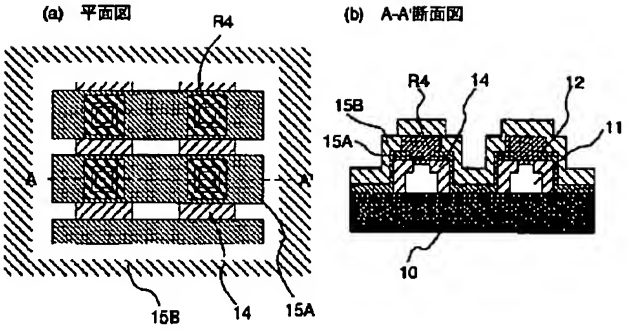
[Drawing 12]

図12



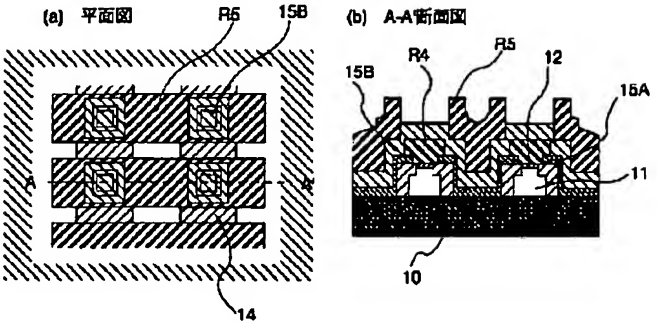
[Drawing 13]

図13



[Drawing 14]

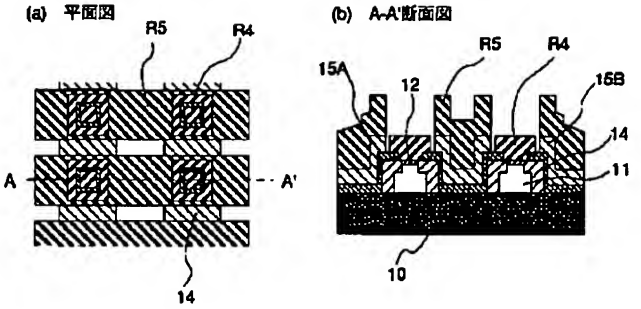
図14



[Drawing 15]

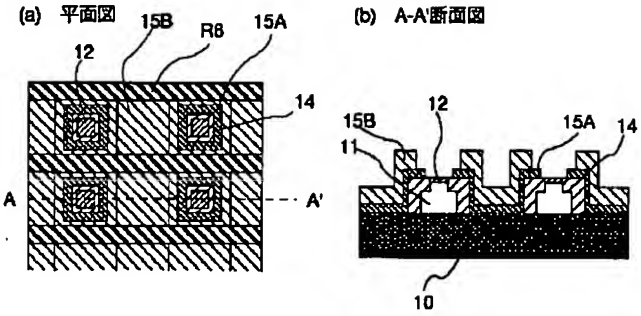
h g cg b eb cg e e

図15



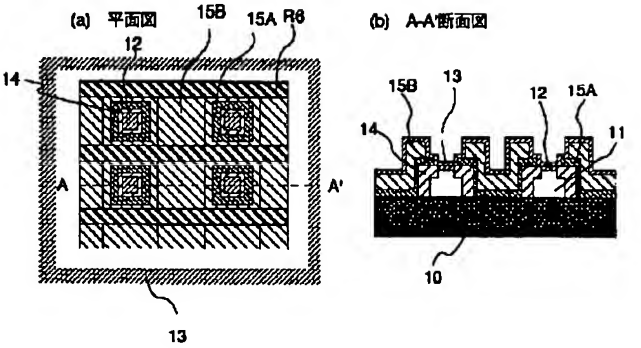
[Drawing 16]

図16



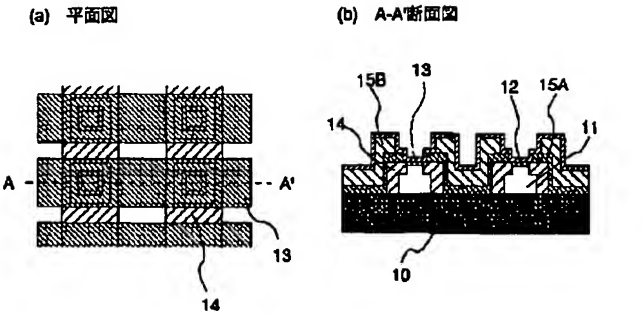
[Drawing 17]

図17



[Drawing 18]

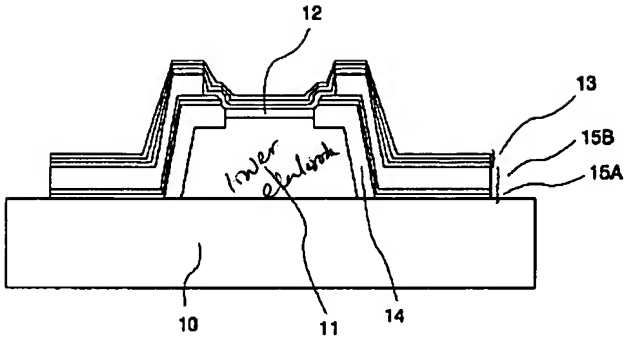
図18



[Drawing 19]

h g cg b eb cg e e

図19

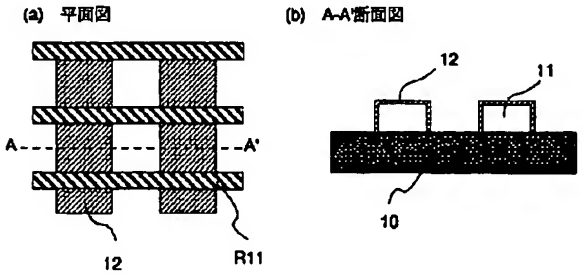


[Drawing 20]

図20

[Drawing 21]

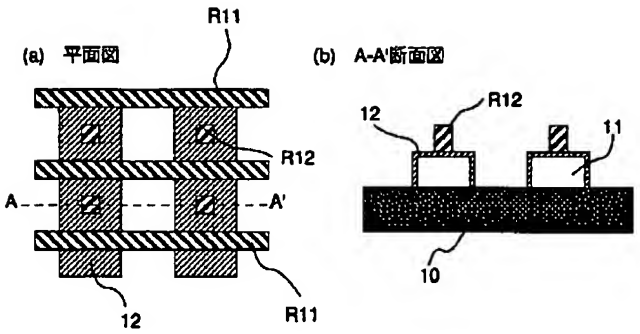
図21



[Drawing 22]

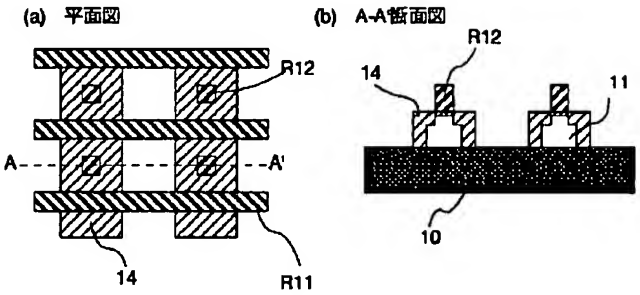
h g cg b eb cg e e

図22



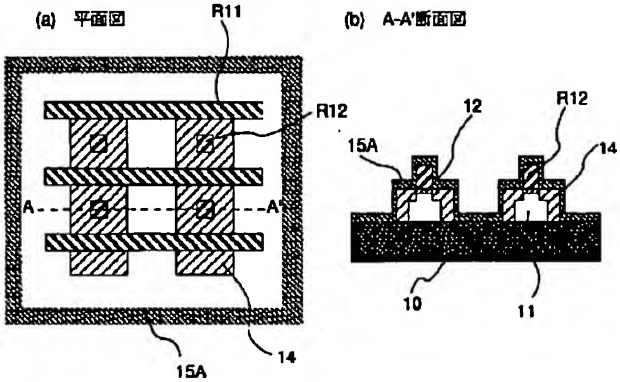
[Drawing 23]

図23



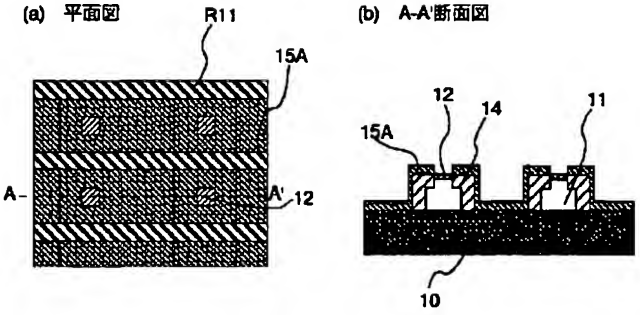
[Drawing 24]

図24.



[Drawing 25]

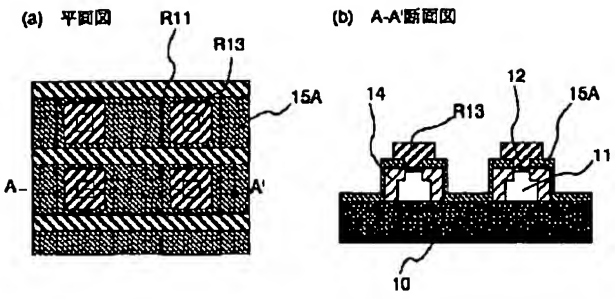
図25



[Drawing 26]

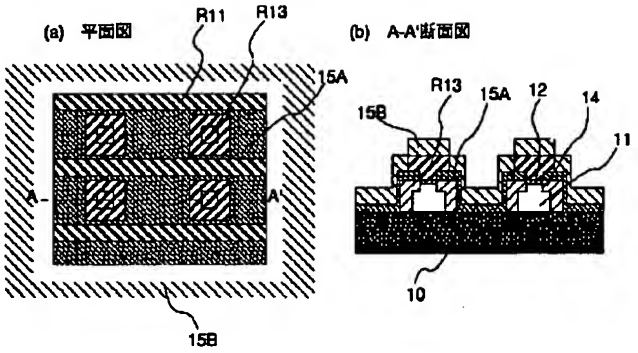
h g cg b eb cg e e

図26



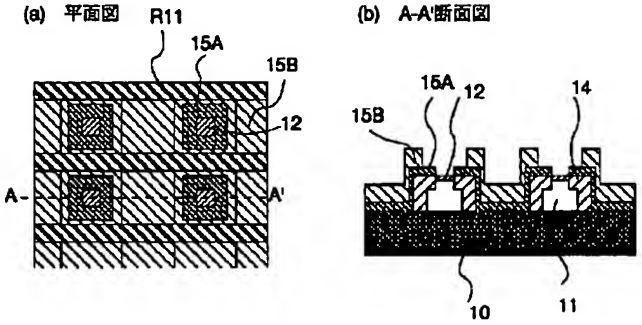
[Drawing 27]

図27



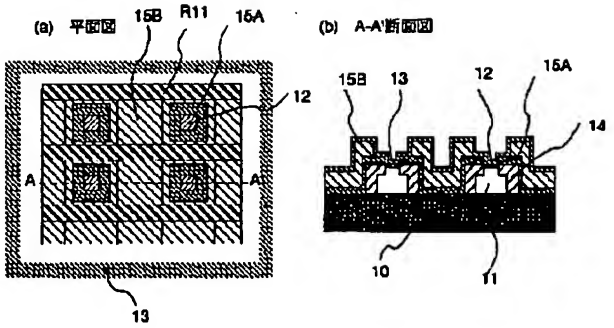
[Drawing 28]

図28



[Drawing 29]

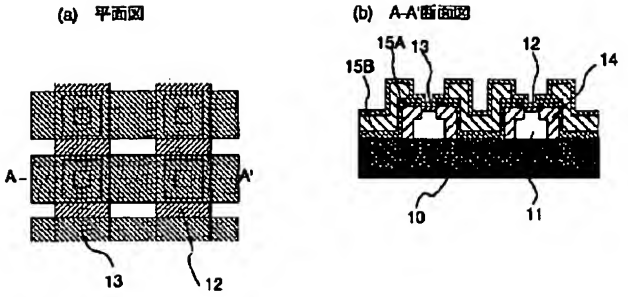
図29



[Drawing 30]

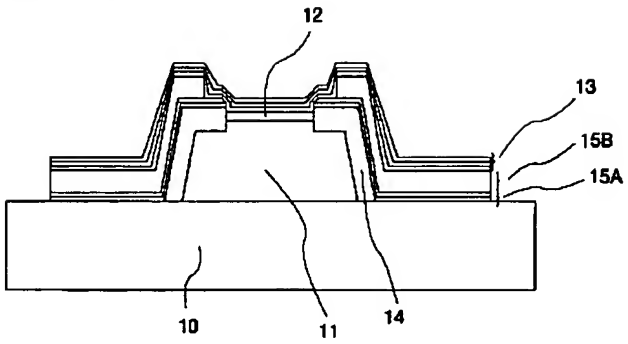
h g cg b eb cg e e

図30



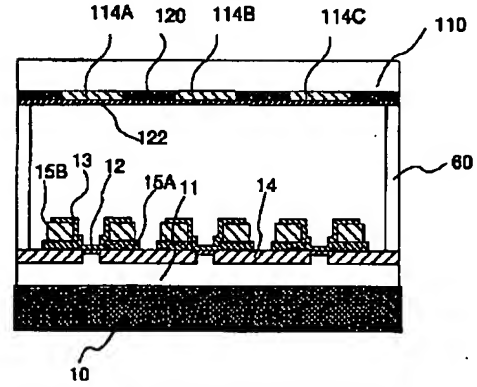
[Drawing 31]

図31



[Drawing 32]

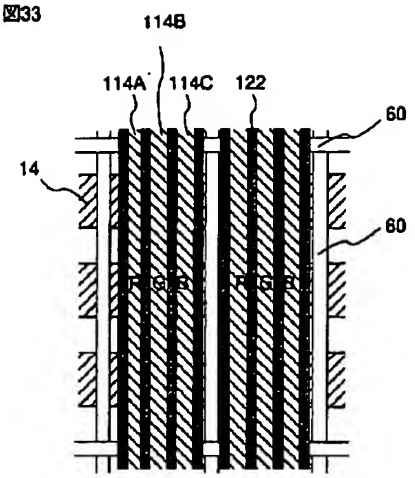
図32



[Drawing 33]

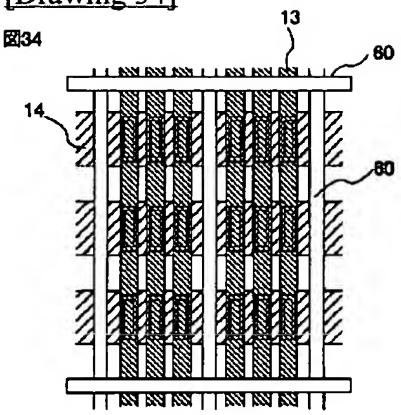
h g cg b eb cg e e

図33



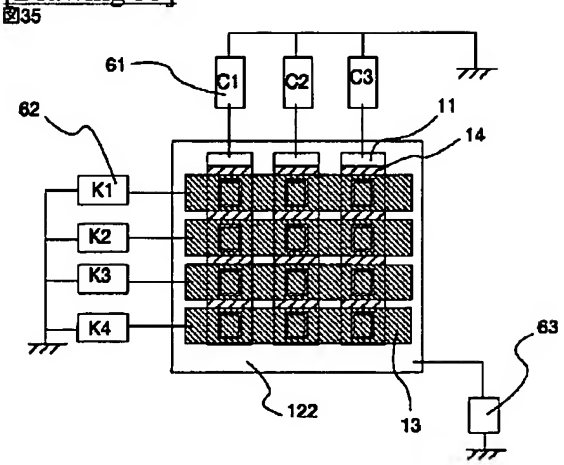
[Drawing 34]

図34



[Drawing 35]

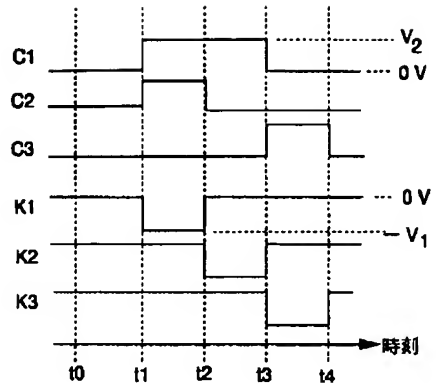
図35



[Drawing 36]

h g cg b eb cg e e

図38



[Translation done.]

h g cg b eb cg e e